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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,466	02/07/2001	Mark Phillips	S1022/8618	5904

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EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	10

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,466	PHILLIPS, MARK	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Response to arguments*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Weaver Johnson et al. U.S. Patent 6,173,421.

As per claim 1, Weaver Johnson ("Johnson") teaches a method of debugging a target system using a host system connected thereto (column 7, lines 8-14; column 8, lines 4-32) comprising a digital signal processor having associated memory comprising plural addressable locations (column 7, lines 15-43), said target system further having a reserved storage location designated as a vector (column 7, lines 48-53, wherein, the call stack of the Johnson is equivalent to the vector of the present application), said memory further storing a plurality of application programs (column 7, lines 43-54; column 6, lines 42-46), each application program having respective associated exception handler code (column 3, lines 34-40), the method comprising: dynamically loading a stack to a reserved region of said memory (column 3, lines 43-46; column 9, line 50 – column 10, line 11, wherein, the central stack is equivalent to the stack of the present application); causing the vector of said target system to point to said stack (column 10, lines 63-

66, wherein, the call stack points to the central stack), whereby all said application programs use the said stack for a particular exception (column 9, line 30 – column 10, line 11).

As per claim 2, Johnson teaches the method of claim 1 further comprising the steps of: dynamically loading a library (column 9, lines 50-63) to said target from said host (column 7, lines 8-14) whereby said dynamically loaded library has an entry point at one of said plural addressable locations (column 9, line 50 – column 10, line 11), wherein said library includes at least one routine needed for running at least one of said applications (column 4, lines 14-25); and storing information indicative of the address of said one location at a reserved location in said stack (column 10, lines 63-66).

As per claim 3, Johnson teaches the method of claim 2 further comprising the step of: using said host to start of one of said applications (column 7, lines 8-14), whereby a running application identifies the need for said routine (column 4, lines 15-19); reading said vector; using the contents of the vector to access said stack (column 10, lines 63-66); reading said reserved stack location to derive the entry point of said library to said application; calling said routine from said library (column 9, line 30 – column 10, line 11).

As per claim 5, Johnson teaches the method of claim 3 wherein said routine comprises a routine enabling a hardware bug to be worked round (column 3, line 52 – column 4, line 14).

As per claim 6, Johnson teaches the method of claim 3 wherein said step of calling comprises supplying a first item of data indicative of the routine and a second item of data for the operation to be performed by said routine (column 9, line 30 – column 10, line 66).

As per claim 7, Johnson teaches the method of claim 6 wherein said routine returns an item of data to said application (column 9, line 30 – column 10, line 66).

As per claim 8, Johnson teaches the method of claim 6 wherein each said data item comprises a machine word (column 17, lines 4-21).

As per claim 9, Johnson teaches device for debugging a target system, the device comprising a host system connected thereto (column 7, lines 8-14; column 8, lines 4-32), the target system comprising a digital signal processor having associated memory comprising a plurality of addressable locations (column 7, lines 15-43), said target system further having a reserved storage location designated as a vector (column 7, lines 48-53), said memory further storing a plurality of application programs (column 7, lines 43-54), each application program having respective associated exception handler code (column 3, lines 34-40), the device further comprising: stack dynamic loading circuitry in said host system for dynamically loading a stack to a reserved region of said memory (column 3, lines 43-46; column 9, line 50 – column 10, line 11), whereby said loading circuitry comprises an indication of the location in said memory of said stack; and vector writing circuitry receiving said indication, and writing to said the vector of said target system the address of said stack whereby all said application programs use the said stack for a particular exception (column 9, line 30 – column 10, line 66).

As per claim 10, Johnson teaches the device of claim 9 further comprising: a computer file in said host (column 7, line 8-14), said file comprising a library having a routine needed by at least one of said applications (column 3, lines 34-40; column 9, lines 50-63); library dynamic loading circuitry for dynamically loading said library to said target from said host whereby said dynamically loaded library has an entry point at one of said plural addressable locations (column 3, lines 34-40; column 9, lines 50-63); and stack writing circuitry for storing information

indicative of the address of said one location at a reserved location in said stack (column 4, lines 14-25; column 10, lines 63-66).

As per claim 11, Johnson teaches the device of claim 10 further comprising: control circuitry in said host for starting one of said applications (column 7, lines 8-14), whereby a running application identifies the need for said routine (column 4, lines 15-19); vector reading circuitry in said target for reading the content of said vector; addressing circuitry for using the contents of the vector to access said stack; stack reading circuitry for reading said reserved stack location to derive the entry point of said library to said application; calling circuitry for calling said routine from said library (column 9, line 30 – column 10, line 66).

As per claim 12, Johnson teaches the device of claim 11 wherein said calling circuitry is operable to supply a first item of data indicative of the routine and a second item of data for the operation to be performed by said routine (column 9, line 30 – column 10, line 66).

As per claim 13, Johnson teaches the device of claim 12 wherein each said data item comprises a machine word (column 17, lines 4-20).

Allowable Subject Matter

3. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1-2, 9-10 have been considered but are moot in view of the new ground(s) of rejection. The amended claims are deemed to cite a broader scope than the original claims, and, as such, new rejections are presented.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (703)305-7599. The examiner can normally be reached on M-F, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
June 24, 2004

SCOTT BADERMAN
PRIMARY EXAMINER